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PATENT



IN THE UNITED STATES PATENT & TRADEMARK OFFICE

APPLICANTS: LUK et al. EXAMINER: NGUYEN, Tuan T.
SERIAL NO: 10/735,061 ART UNIT: 2824
FILED: Dec. 11, 2003 DKT: YOR920030136US1 (8728-621)
ON: GATED DIODE MEMORY CELLS

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

RESPONSE TO RESTRICTION REQUIREMENT

This paper is responsive to the Office Action mailed on February 6, 2006, which includes a restriction requirement. The Examiner is requested to enter and consider the following remarks.

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8(a)

I hereby certify that this correspondence (and any document referred to as being attached or enclosed) is being deposited with the United States Postal Service as first class mail, postage paid in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 on the date indicated below:

Date: 3/8/06

By: Patricia A. Gonta
Patricia A. Gonta

The Examiner's withdrawal of the previous restriction requirement, dated October 6, 2005, is gratefully acknowledged. In response to the new restriction requirement, dated February 6, 2006, Applicants elect the claims of Group I (Claim nos. 1-51), which are drawn to gated diode memory cells, without traverse.

All issues raised by the Examiner having been addressed, Applicants earnestly solicit an early and favorable consideration of the present application and elected claims.

Respectfully submitted,

By:


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